FIG. 1

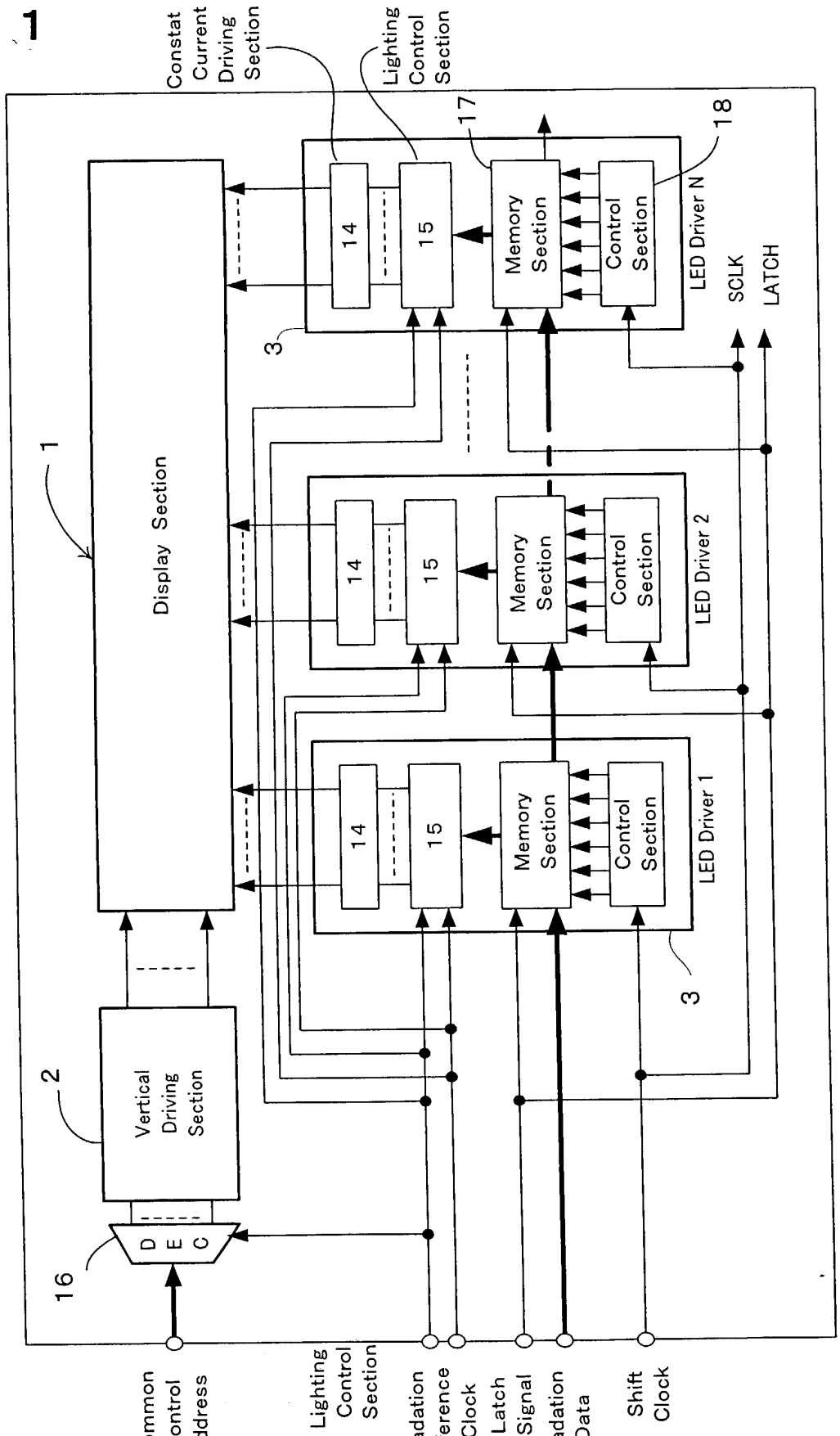

Constat Current Driving Section
Lighting Control Section
17
18
Memory Section
Control Section
LED Driver N
SCLK
LATCH
14
15
3
1
Display Section
LED Driver 2
LED Driver 1
2
Vertical Driving Section
D E C
16
Common Control Address
Lighting Control Section
Gradation Reference Clock
Latch Signal
Gradation Data
Shift Clock

FIG. 2

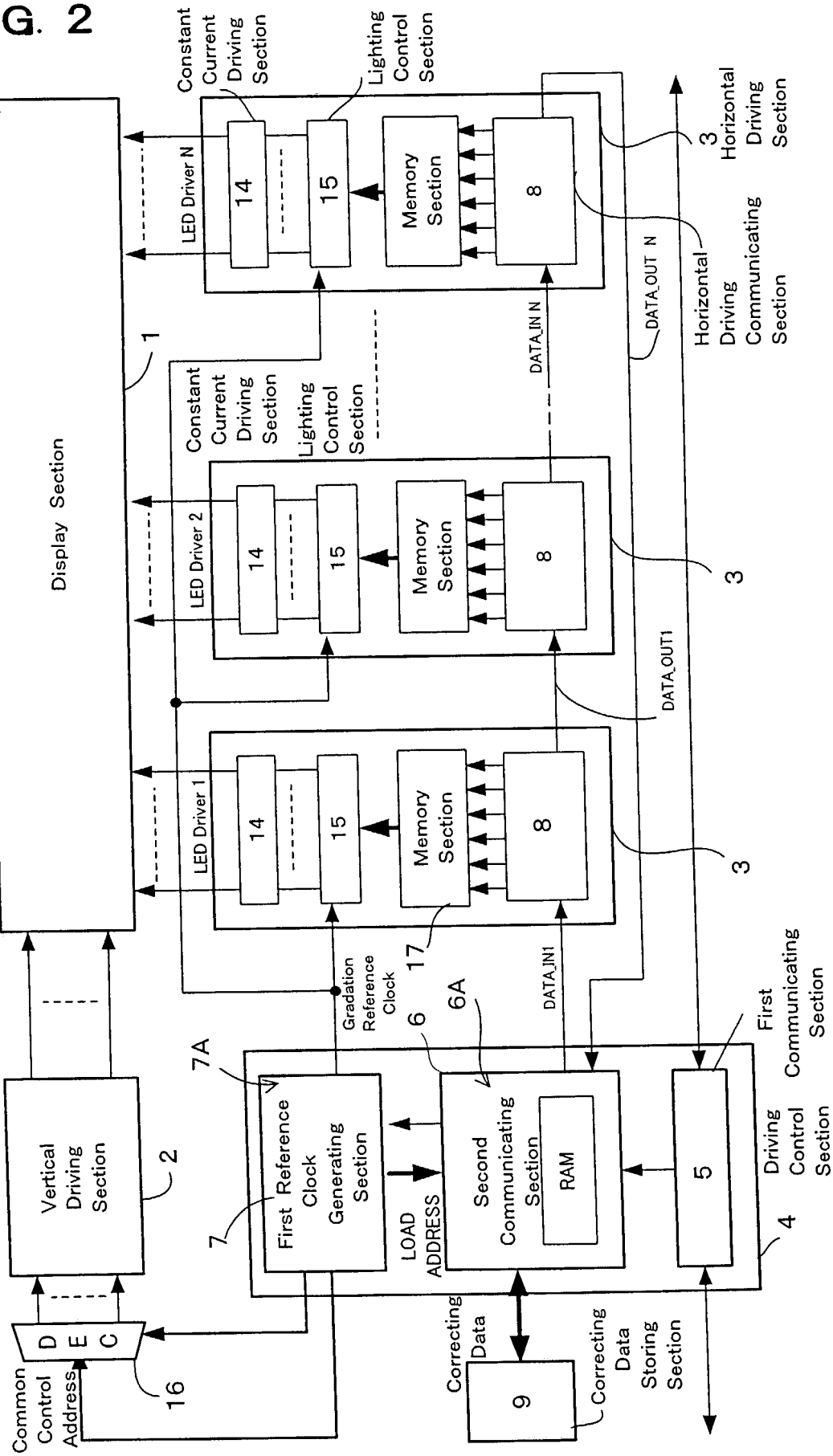

Display Section
1
Vertical Driving Section
2
Horizontal Driving Communicating Section
3
Driving Control Section
4
First Communicating Section
5
6
6A
7
7A
First Reference Clock Generating Section
Second Communicating Section
RAM
LOAD ADDRESS
Gradation Reference Clock
17
DECODER
16
Common Control Address
Correcting Data
9
Correcting Data Storing Section
LED Driver N
LED Driver 2
LED Driver 1
Constant Current Driving Section
Lighting Control Section
14
15
Memory Section
8
DATA_IN N
DATA_OUT N
DATA_IN1
DATA_OUT1
Horizontal Driving Section

FIG. 3

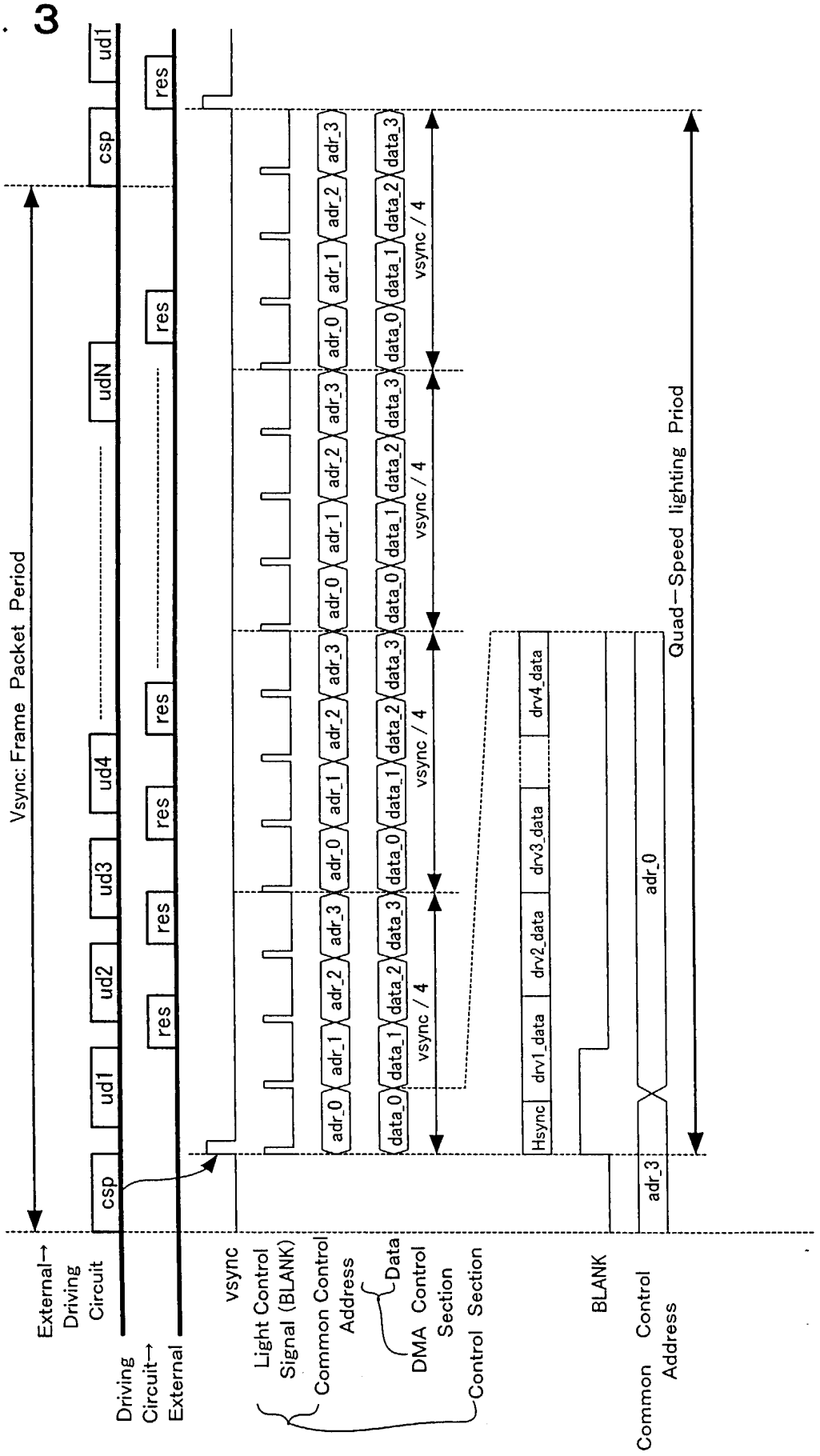

Vsync: Frame Packet Period
External→ Driving Circuit
Driving Circuit→ External
csp
ud1
ud2
ud3
ud4
udN
res
vsync
Light Control Signal (BLANK)
Common Control Address
Data
DMA Control Section
Control Section
adr_0
adr_1
adr_2
adr_3
data_0
data_1
data_2
data_3
vsync / 4
Hsync
drv1_data
drv2_data
drv3_data
drv4_data
BLANK
Common Control Address
Quad-Speed lighting Priod

FIG. 4

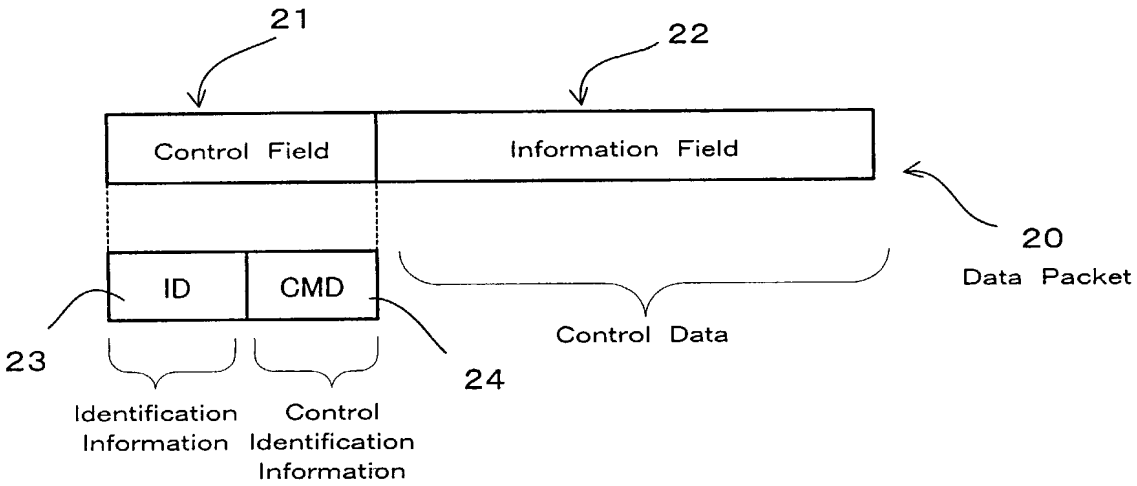

21
22
Control Field
Information Field
20
Data Packet
ID
CMD
23
24
Control Data
Identification Information
Control Identification Information

FIG. 5

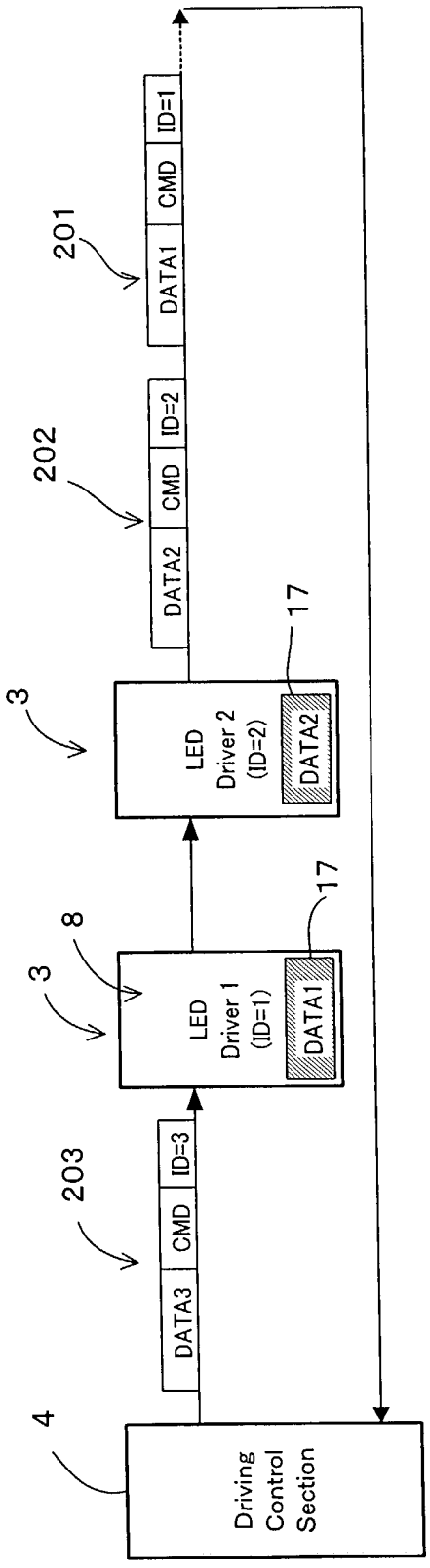

201
DATA1
CMD
ID=1
202
DATA2
CMD
ID=2
17
3
LED
Driver 2
(ID=2)
DATA2
8
3
LED
Driver 1
(ID=1)
DATA1
17
203
DATA3
CMD
ID=3
4
Driving
Control
Section

FIG. 6

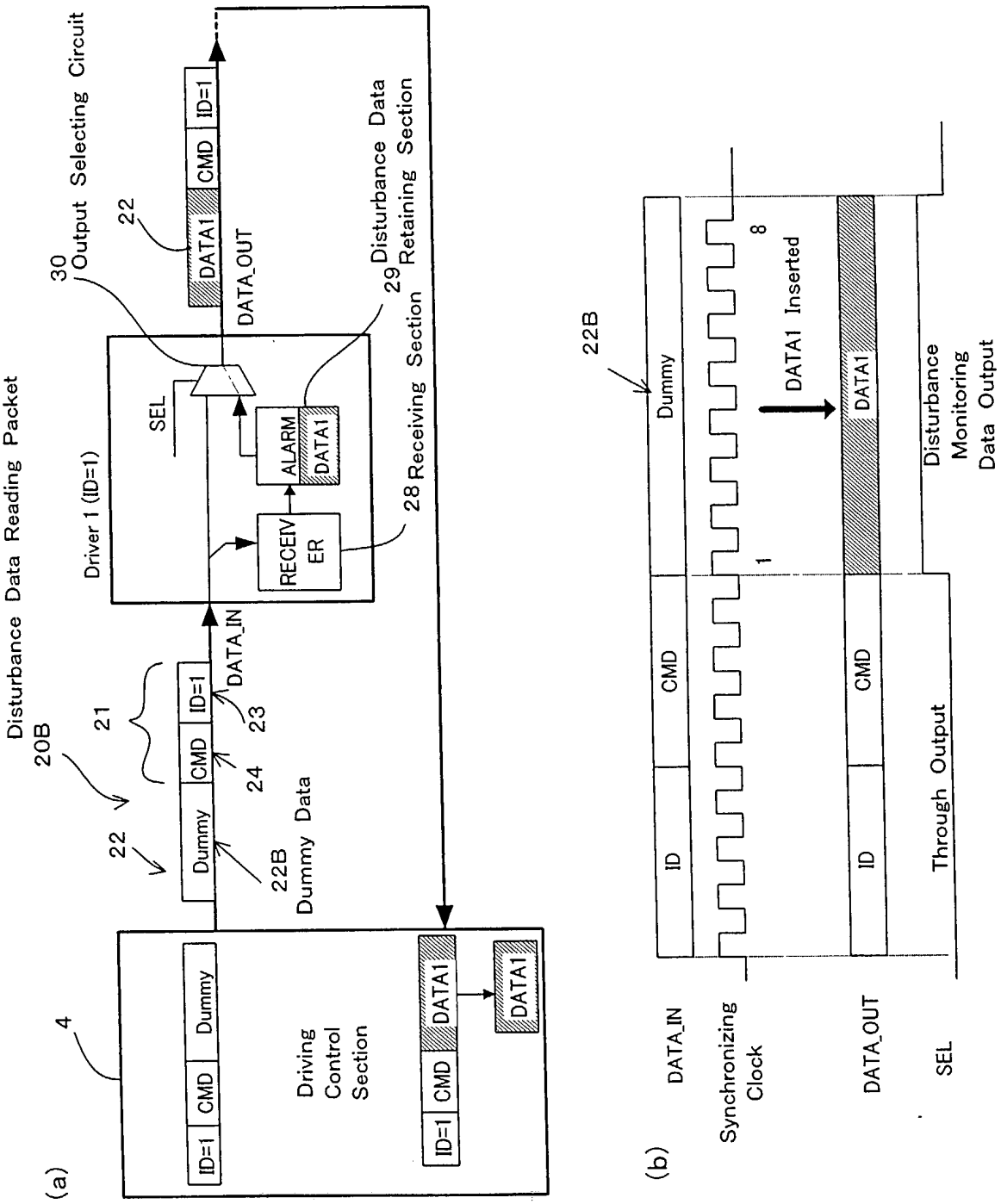

(a)
Disturbance Data Reading Packet
20B
21
22
22B
Dummy Data
Dummy
CMD
ID=1
24
23
DATA_IN
4
Driving Control Section
ID=1
CMD
DATA1
DATA1
Driver 1 (ID=1)
SEL
30
Output Selecting Circuit
RECEIV ER
ALARM
DATA1
28 Receiving Section
29 Disturbance Data Retaining Section
22
DATA1
CMD
ID=1
DATA_OUT
(b)
22B
Dummy
ID
CMD
1
8
DATA1 Inserted
DATA1
Disturbance Monitoring Data Output
DATA_IN
Synchronizing Clock
DATA_OUT
SEL
Through Output

FIG. 7

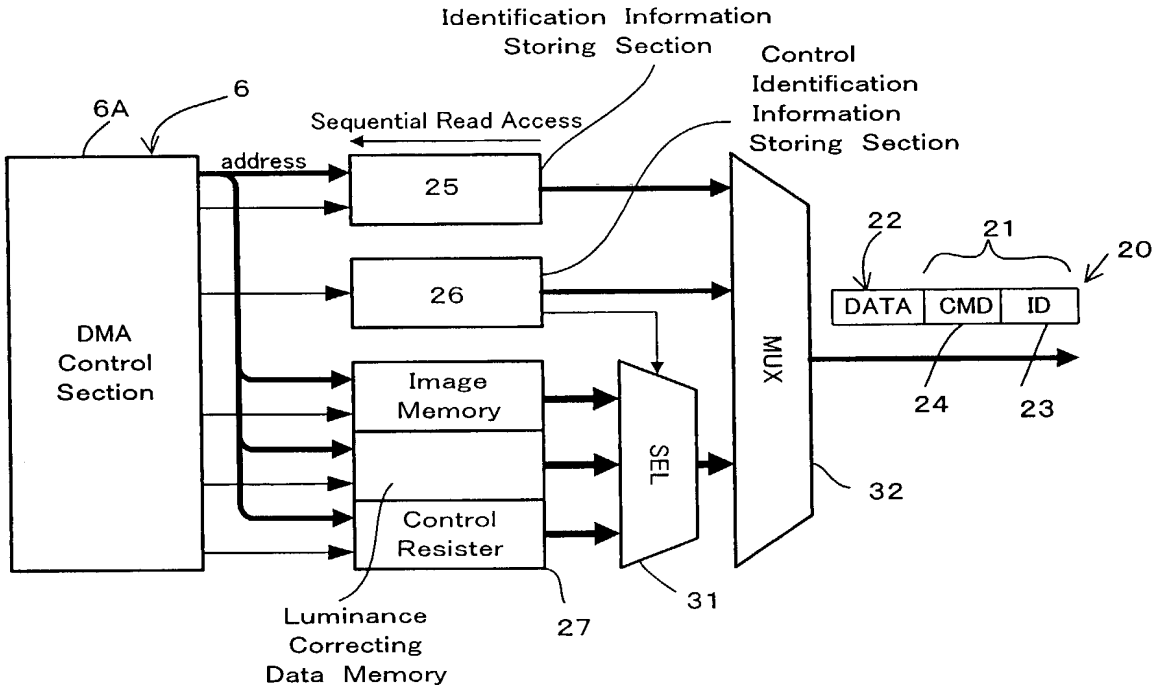
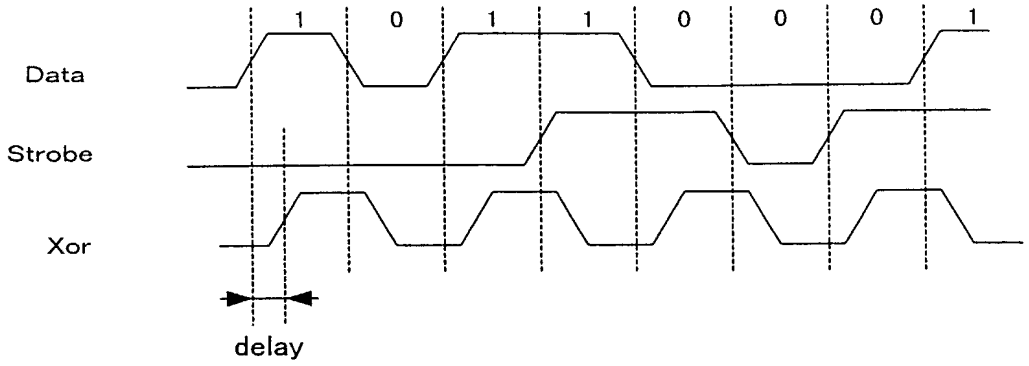
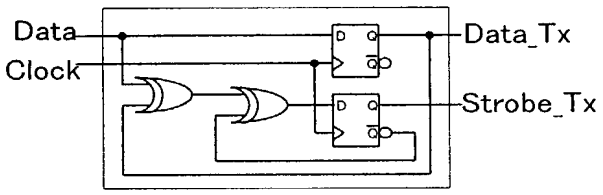

Identification Information Storing Section
Control Identification Information Storing Section
6A
6
Sequential Read Access
address
25
26
DMA Control Section
Image Memory
Control Resister
SEL
MUX
22
21
20
DATA
CMD
ID
24
23
32
31
27
Luminance Correcting Data Memory

FIG. 8 (a)


1
0
1
1
0
0
0
1
Data
Strobe
Xor
delay

(b)


Data
Clock
Data_Tx
Strobe_Tx

(c)

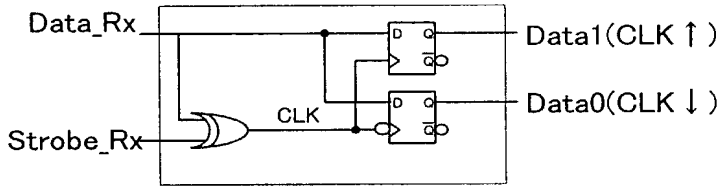

Data_Rx
Strobe_Rx
CLK
Data1(CLK ↑)
Data0(CLK ↓)

FIG. 9

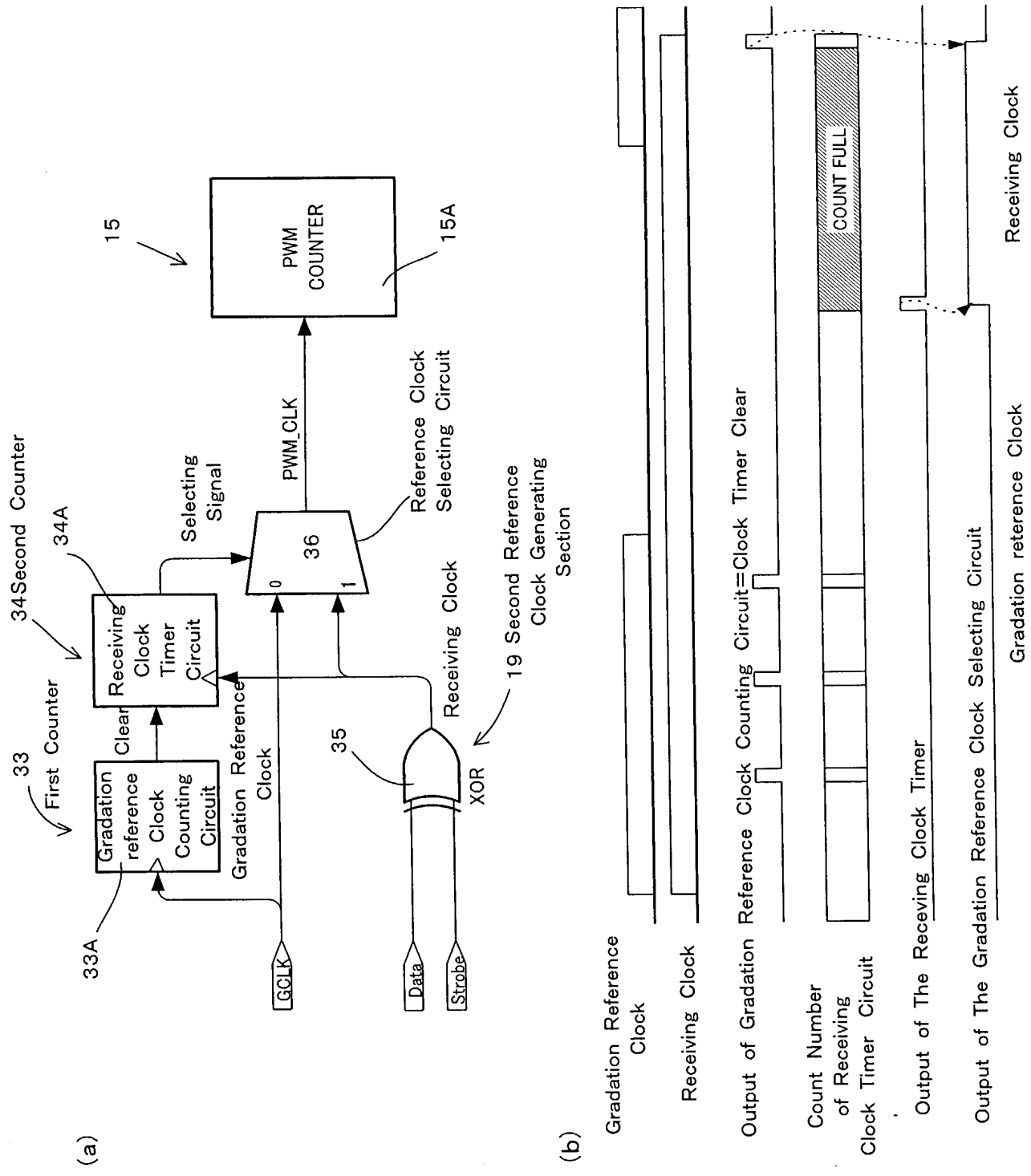

(a)
15
PWM COUNTER
15A
PWM_CLK
Reference Clock Selecting Circuit
36
0
1
Selecting Signal
34Second Counter
34A
Receiving Clock Timer Circuit
Clear
Receiving Clock
19 Second Reference Clock Generating Section
33
First Counter
Gradation reference Clock Counting Circuit
Gradation Reference Clock
35
XOR
33A
GCLK
Data
Strobe
(b)
Gradation Reference Clock
Receiving Clock
Output of Gradation Reference Clock Counting Circuit=Clock Timer Clear
Count Number of Receiving Clock Timer Circuit
COUNT FULL
Output of The Receving Clock Timer
Output of The Gradation Reference Clock Selecting Circuit
Receiving Clock
Gradation reterence Clock

FIG. 10

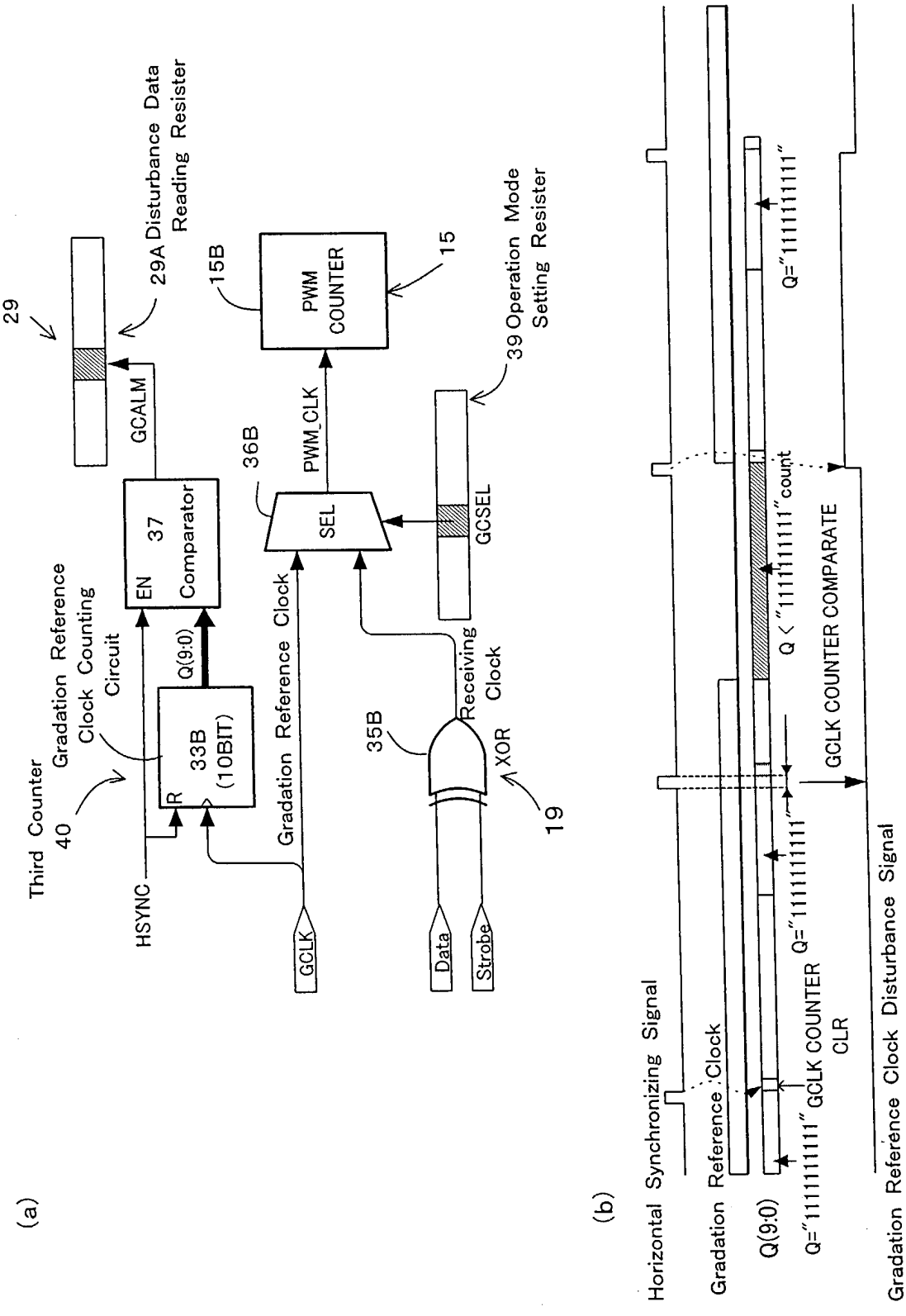

(a)
Third Counter
40
Gradation Reference Clock Counting Circuit
HSYNC
R
33B (10BIT)
Q(9:0)
EN
37 Comparator
GCALM
29
29A Disturbance Data Reading Resister
Gradation Reference Clock
GCLK
36B
SEL
PWM_CLK
15B
PWM COUNTER
15
39 Operation Mode Setting Resister
GCSEL
35B
Receiving Clock
XOR
19
Data
Strobe
(b)
Horizontal Synchronizing Signal
Gradation Reference :Clock
Q(9:0)
Q="1111111111" GCLK COUNTER CLR
Q="1111111111"
Q < "1111111111" count
Q="1111111111"
GCLK COUNTER COMPARATE
Gradation Reference Clock Disturbance Signal

FIG. 11

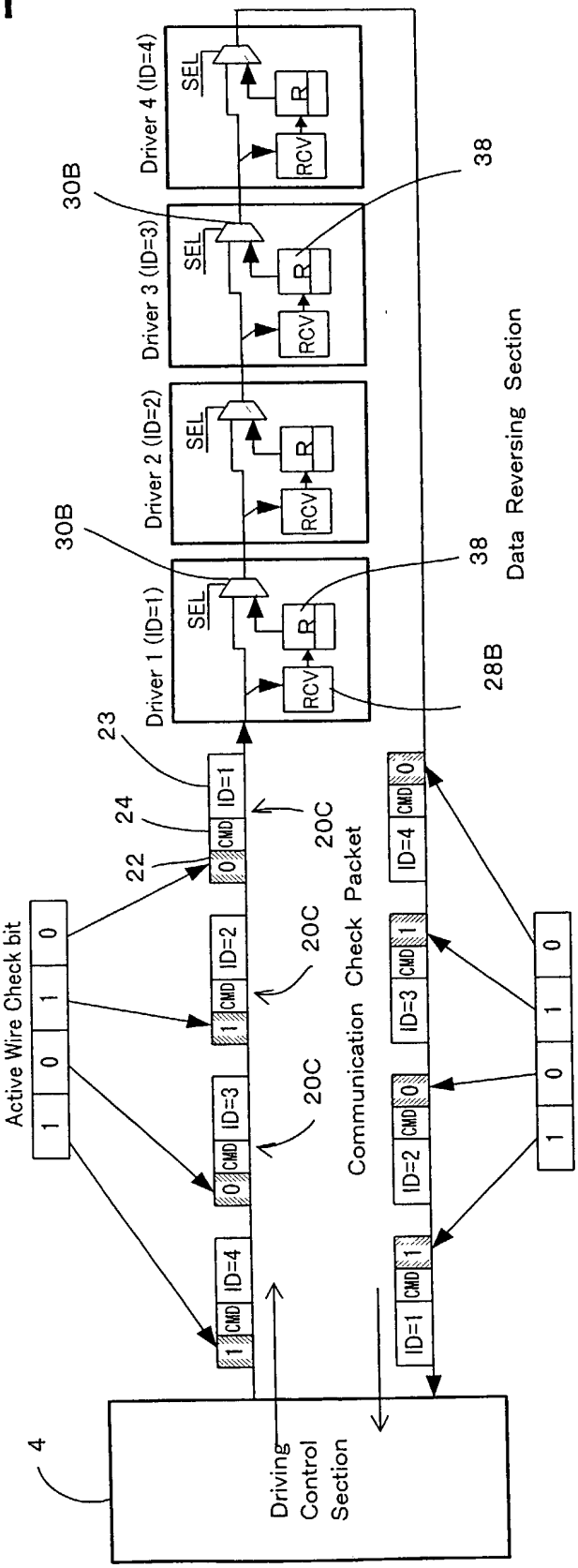
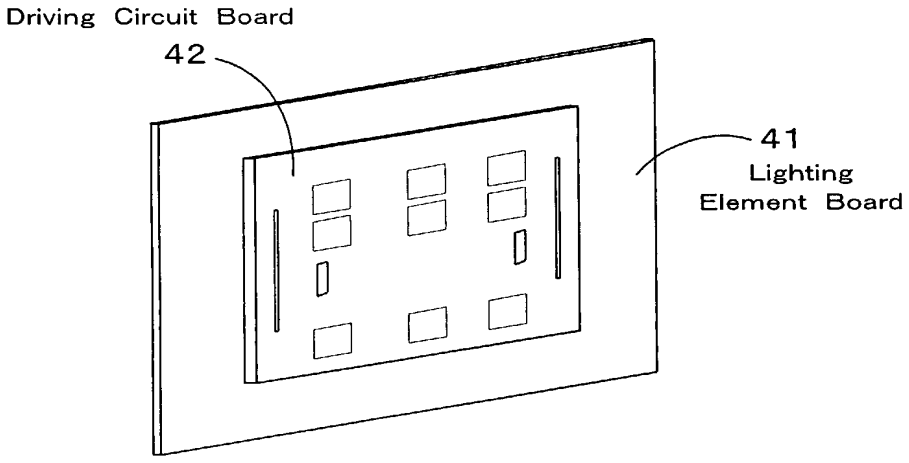

Driver 4 (ID=4)
Driver 3 (ID=3)
Driver 2 (ID=2)
Driver 1 (ID=1)
SEL
RCV
R
30B
38
28B
Data Reversing Section
Active Wire Check bit
Communication Check Packet
20C
22
23
24
CMD
ID=1
ID=2
ID=3
ID=4
Driving Control Section
4

FIG. 12

(a)


Driving Circuit Board
42
41
Lighting
Element Board

(b)

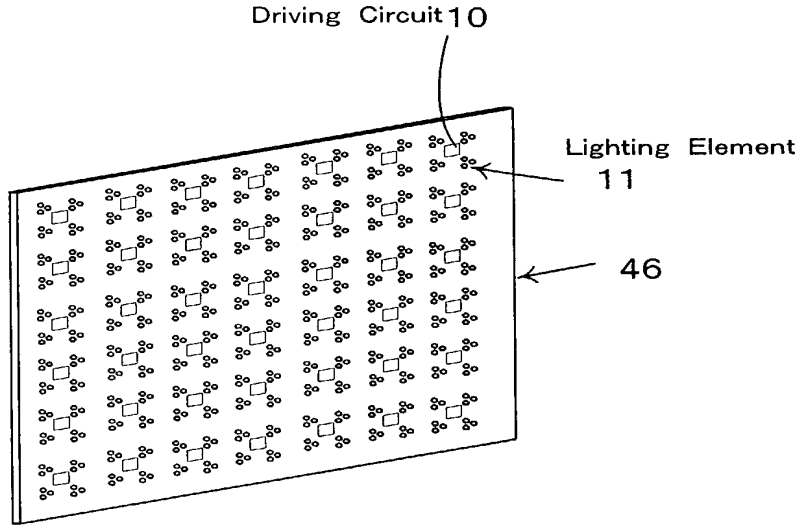

Driving Circuit 10
Lighting Element
11
46

FIG. 13

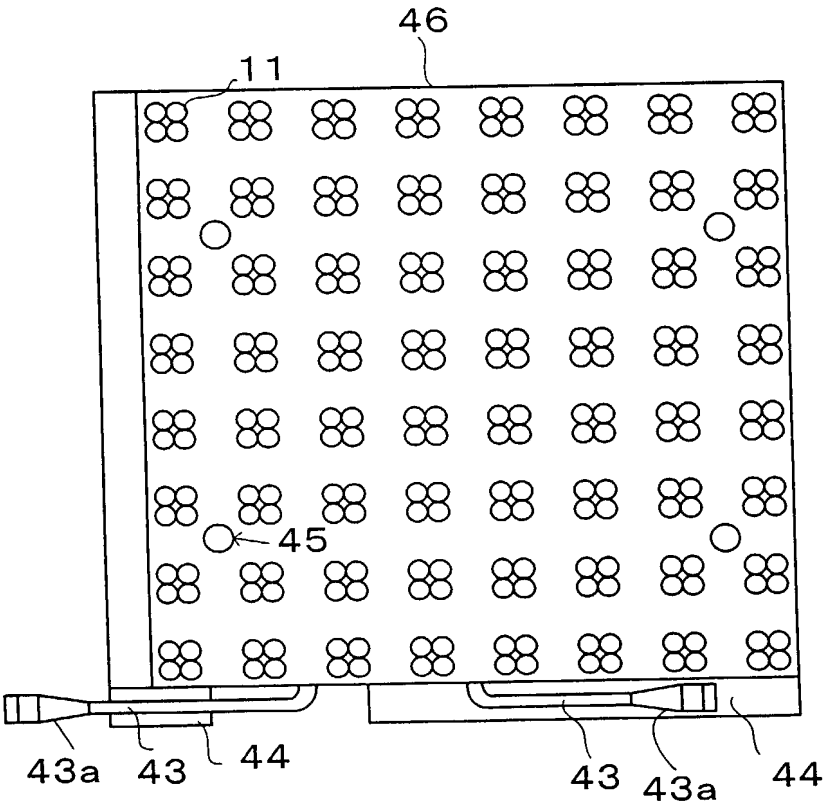


FIG. 14

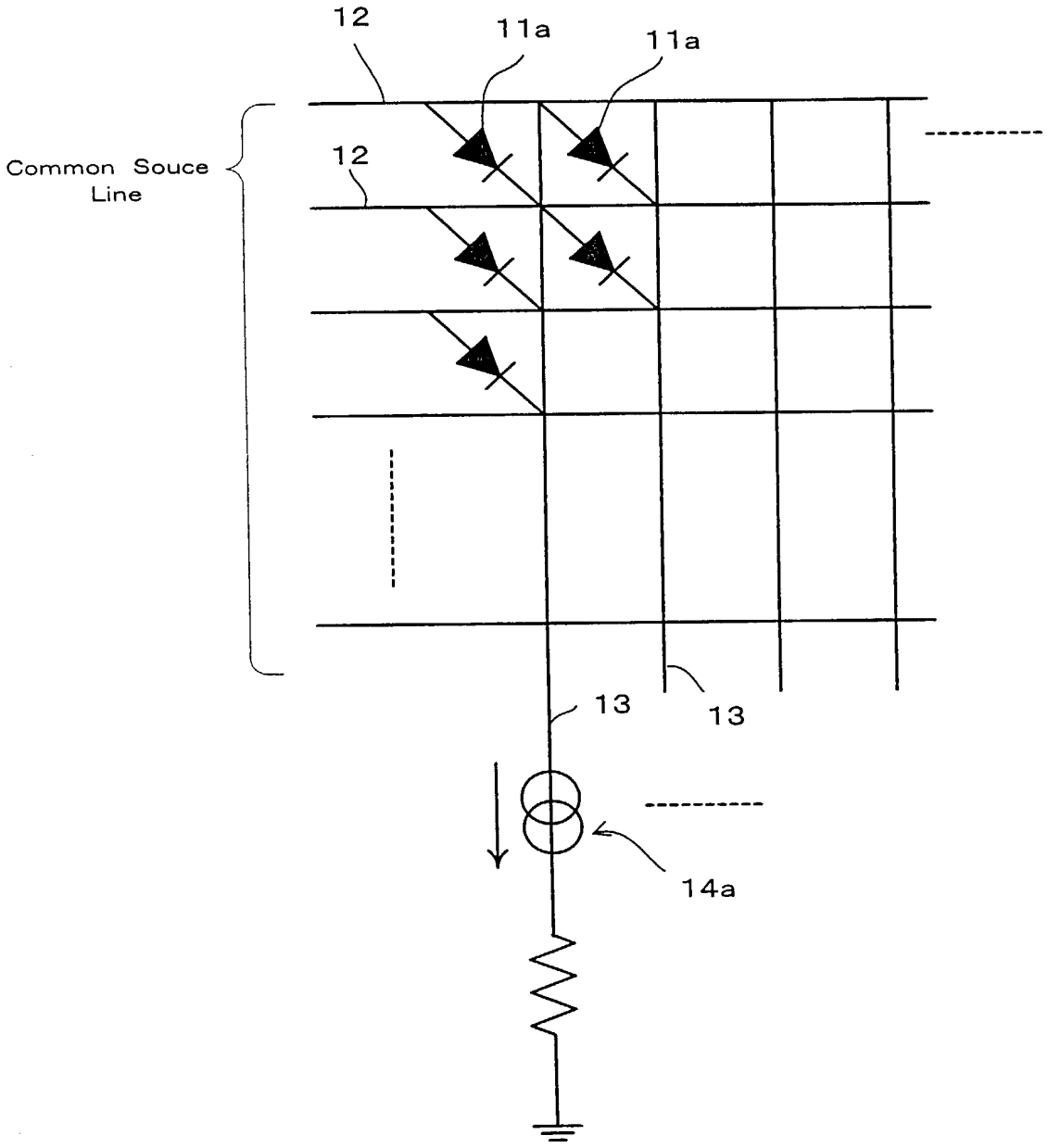


FIG. 15

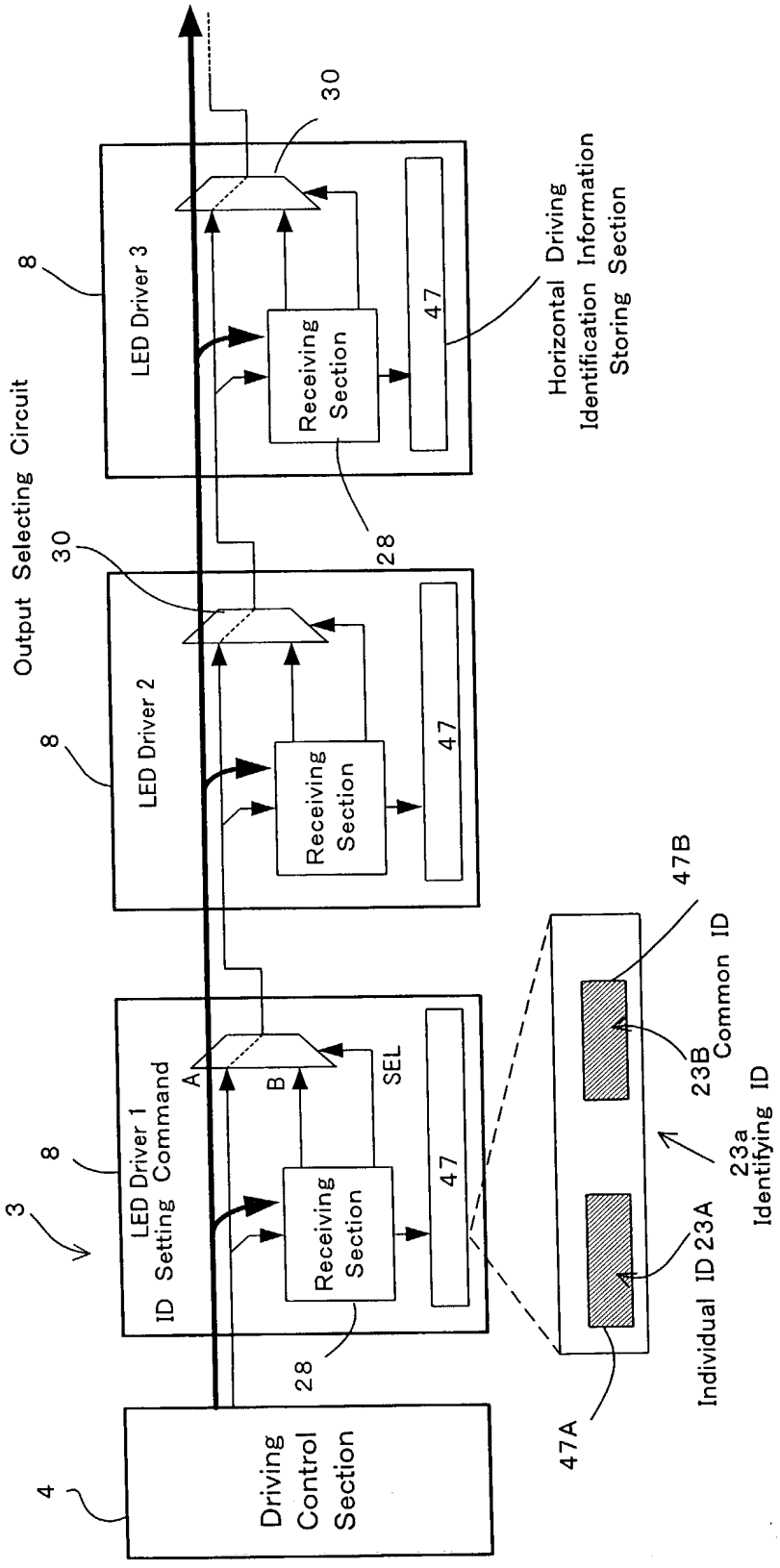

Driving Control Section
4
3
LED Driver 1
ID Setting Command
8
A
B
SEL
Receiving Section
47
28
LED Driver 2
30
Output Selecting Circuit
LED Driver 3
Horizontal Driving Identification Information Storing Section
47B
23B
Common ID
23a
Identifying ID
Individual ID 23A
47A

FIG. 16

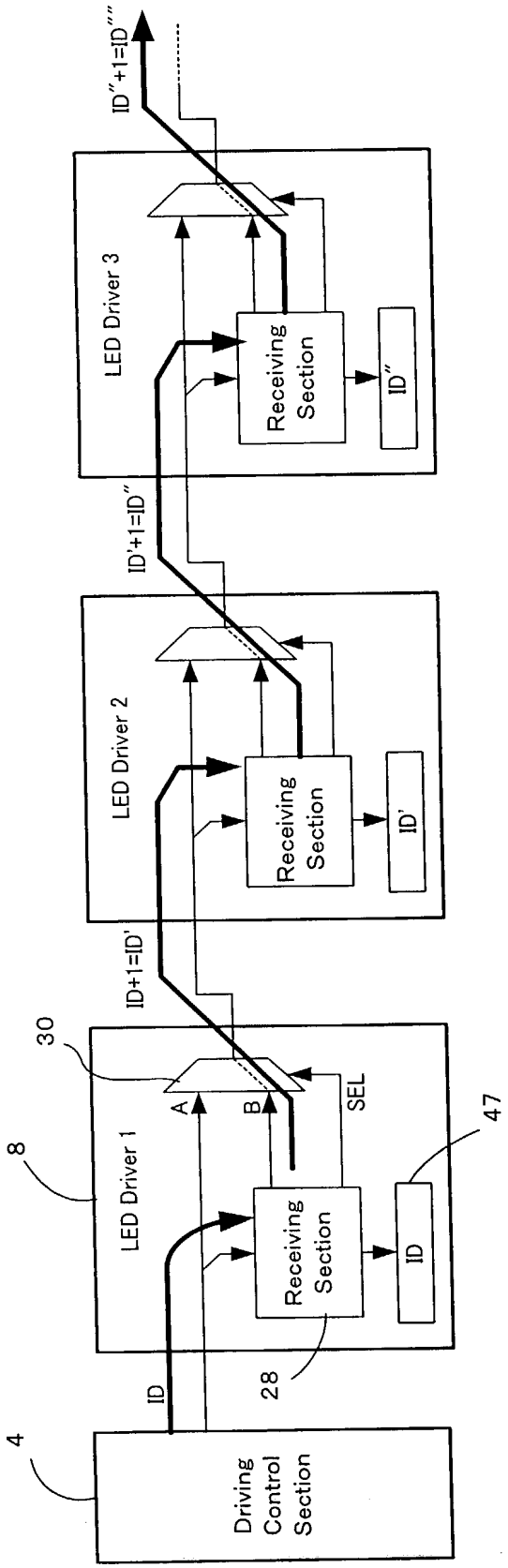

ID"+1=ID'''
LED Driver 3
Receiving Section
ID"
ID'+1=ID"
LED Driver 2
Receiving Section
ID'
ID+1=ID'
30
A
B
SEL
47
8
LED Driver 1
Receiving Section
ID
28
ID
4
Driving Control Section

FIG. 17

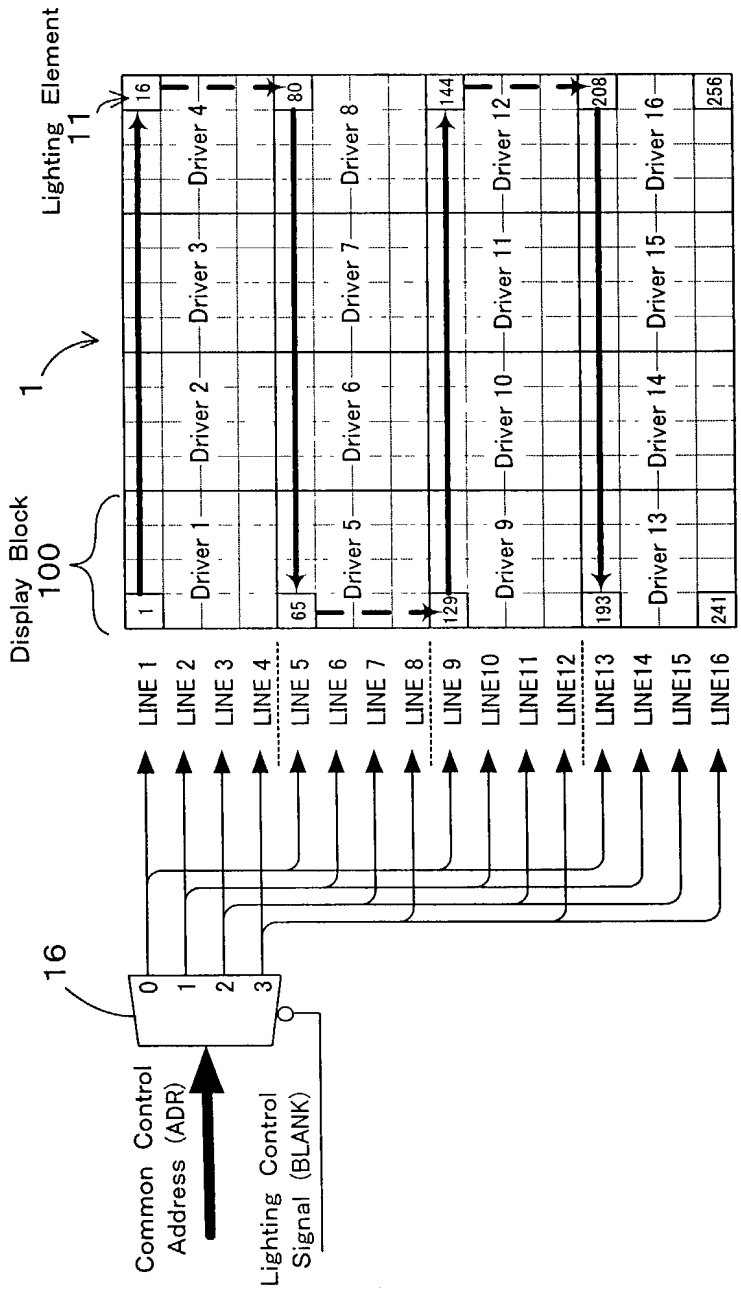

Lighting Element
11
1
Display Block
100
Driver 1
Driver 2
Driver 3
Driver 4
Driver 5
Driver 6
Driver 7
Driver 8
Driver 9
Driver 10
Driver 11
Driver 12
Driver 13
Driver 14
Driver 15
Driver 16
1
16
65
80
129
144
193
208
241
256
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
LINE10
LINE11
LINE12
LINE13
LINE14
LINE15
LINE16
16
0
1
2
3
Common Control
Address (ADR)
Lighting Control
Signal (BLANK)

FIG. 18

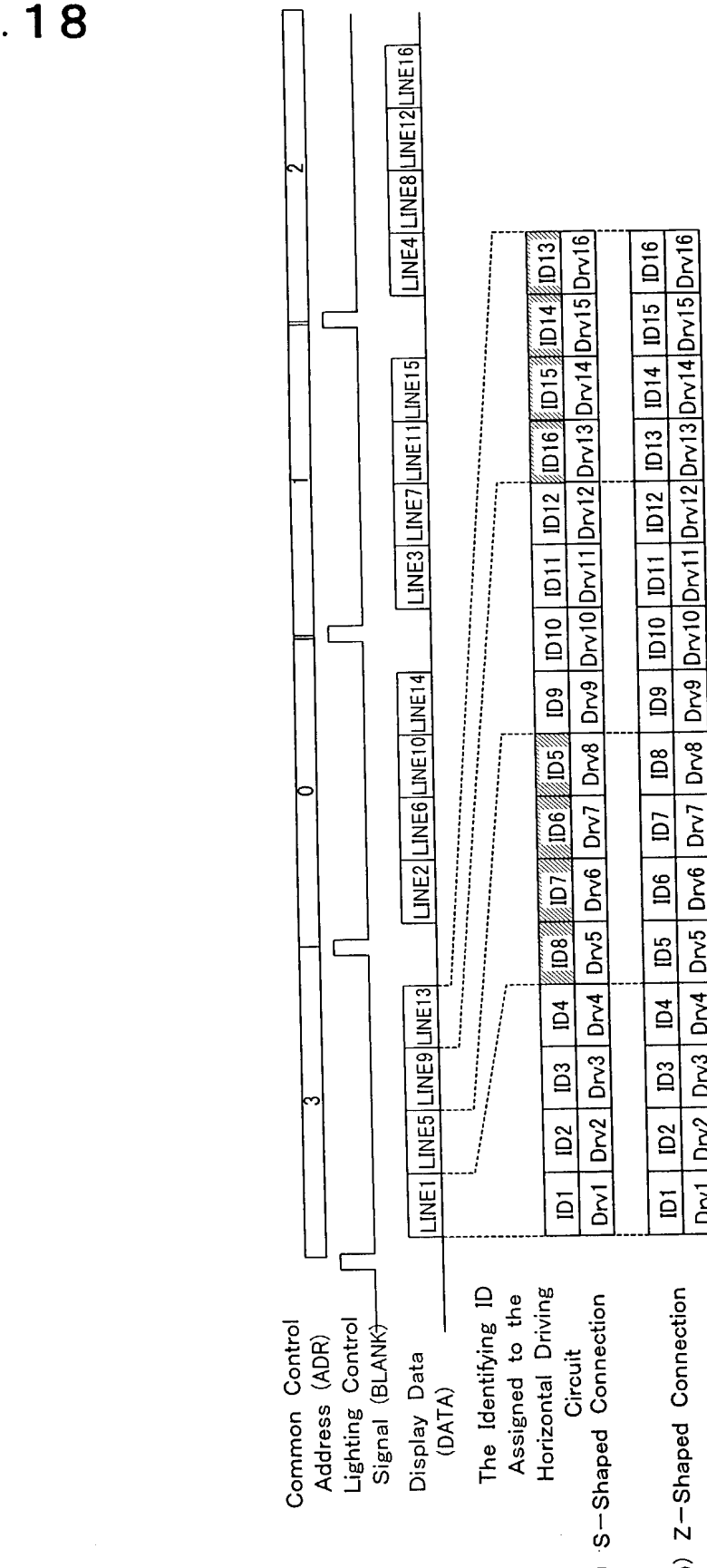

Common Control Address (ADR)
Lighting Control Signal (BLANK)
Display Data (DATA)
The Identifying ID Assigned to the Horizontal Driving Circuit
(a) S-Shaped Connection
(b) Z-Shaped Connection
0
1
2
3
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE9
LINE10
LINE11
LINE12
LINE13
LINE14
LINE15
LINE16
ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13
ID14
ID15
ID16
Drv1
Drv2
Drv3
Drv4
Drv5
Drv6
Drv7
Drv8
Drv9
Drv10
Drv11
Drv12
Drv13
Drv14
Drv15
Drv16

FIG. 19

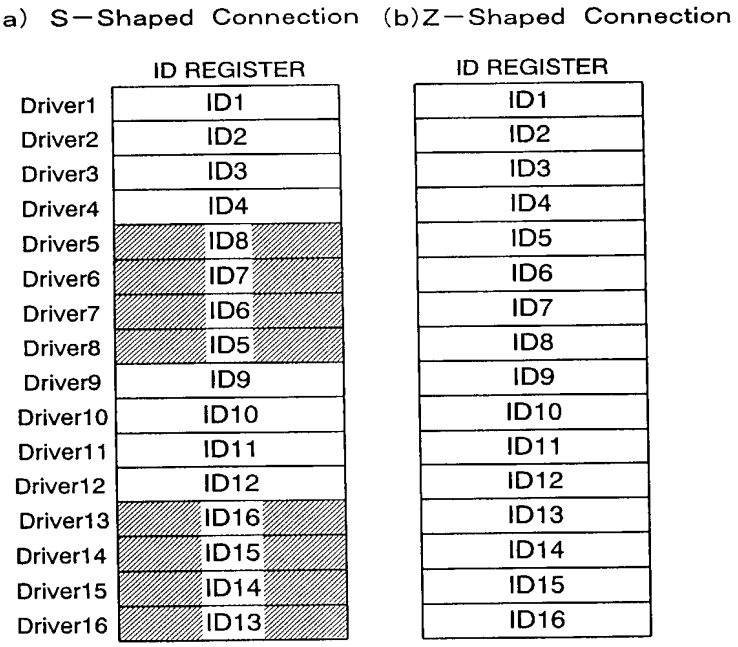

(a) S−Shaped Connection
(b)Z−Shaped Connection
ID REGISTER
Driver1
Driver2
Driver3
Driver4
Driver5
Driver6
Driver7
Driver8
Driver9
Driver10
Driver11
Driver12
Driver13
Driver14
Driver15
Driver16
ID1
ID2
ID3
ID4
ID8
ID7
ID6
ID5
ID9
ID10
ID11
ID12
ID16
ID15
ID14
ID13
ID REGISTER
ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13
ID14
ID15
ID16

FIG. 20

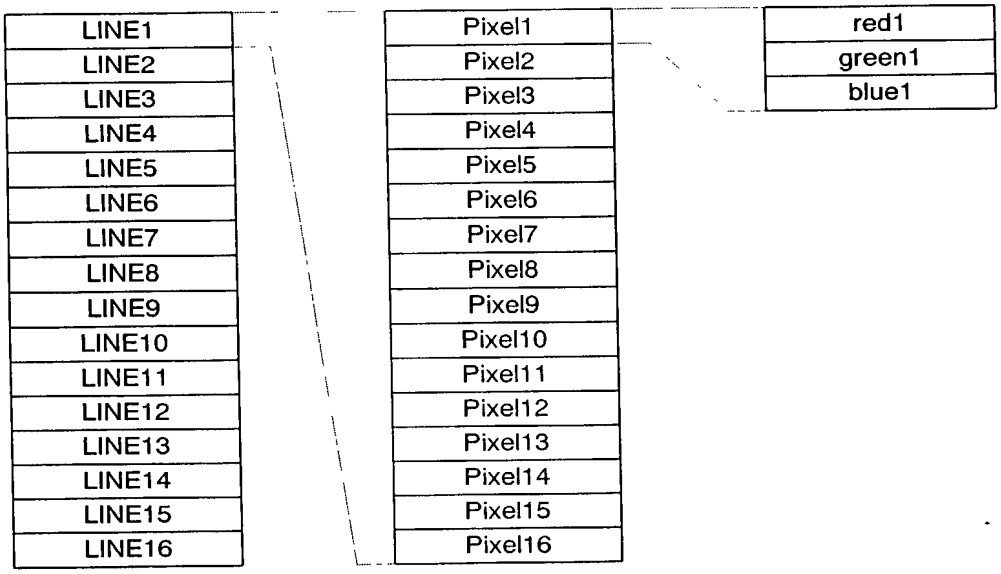

LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE9
LINE10
LINE11
LINE12
LINE13
LINE14
LINE15
LINE16
Pixel1
Pixel2
Pixel3
Pixel4
Pixel5
Pixel6
Pixel7
Pixel8
Pixel9
Pixel10
Pixel11
Pixel12
Pixel13
Pixel14
Pixel15
Pixel16
red1
green1
blue1

FIG. 21

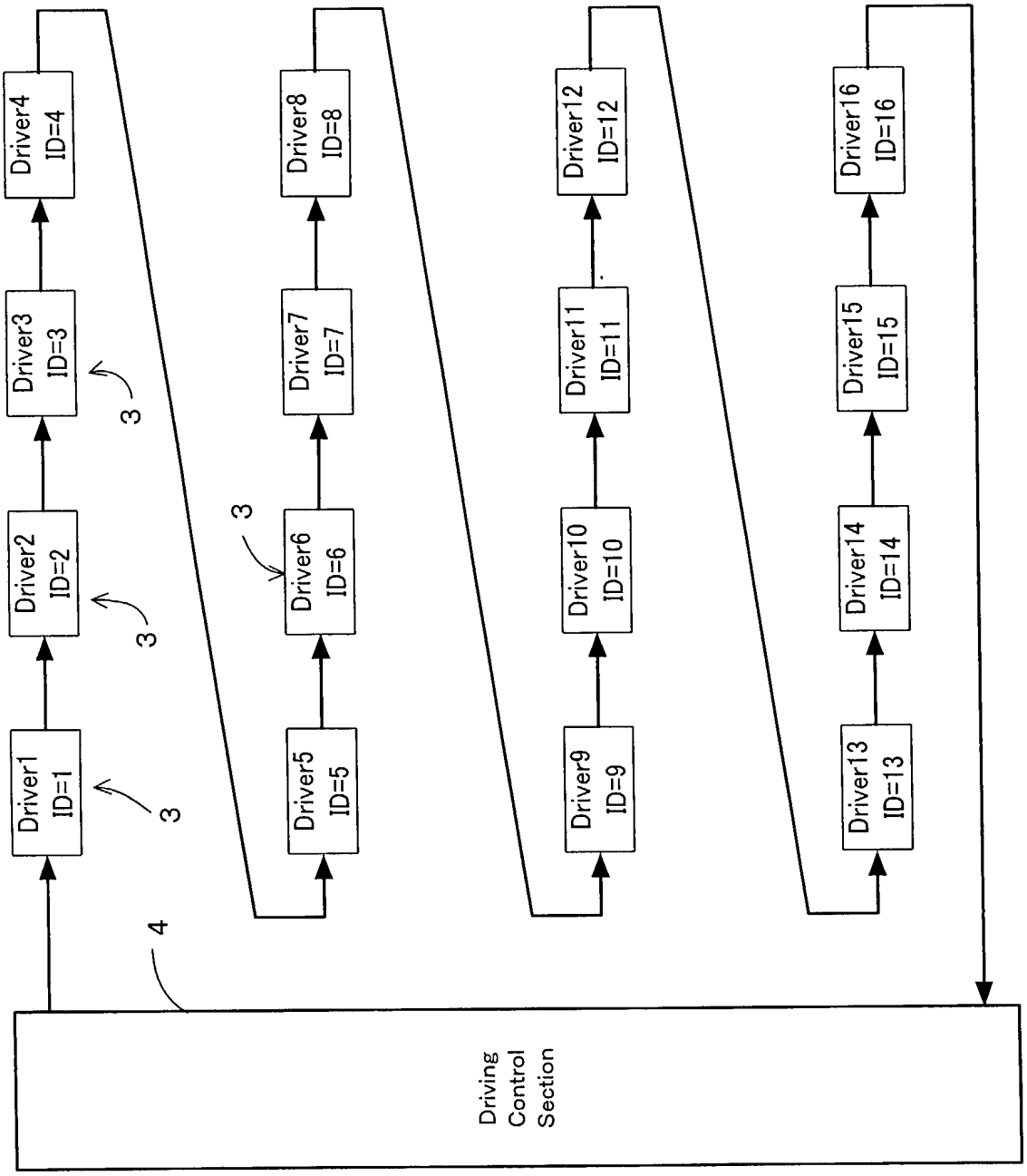

Driver1 ID=1
Driver2 ID=2
Driver3 ID=3
Driver4 ID=4
Driver5 ID=5
Driver6 ID=6
Driver7 ID=7
Driver8 ID=8
Driver9 ID=9
Driver10 ID=10
Driver11 ID=11
Driver12 ID=12
Driver13 ID=13
Driver14 ID=14
Driver15 ID=15
Driver16 ID=16
3
4
Driving Control Section

FIG. 22

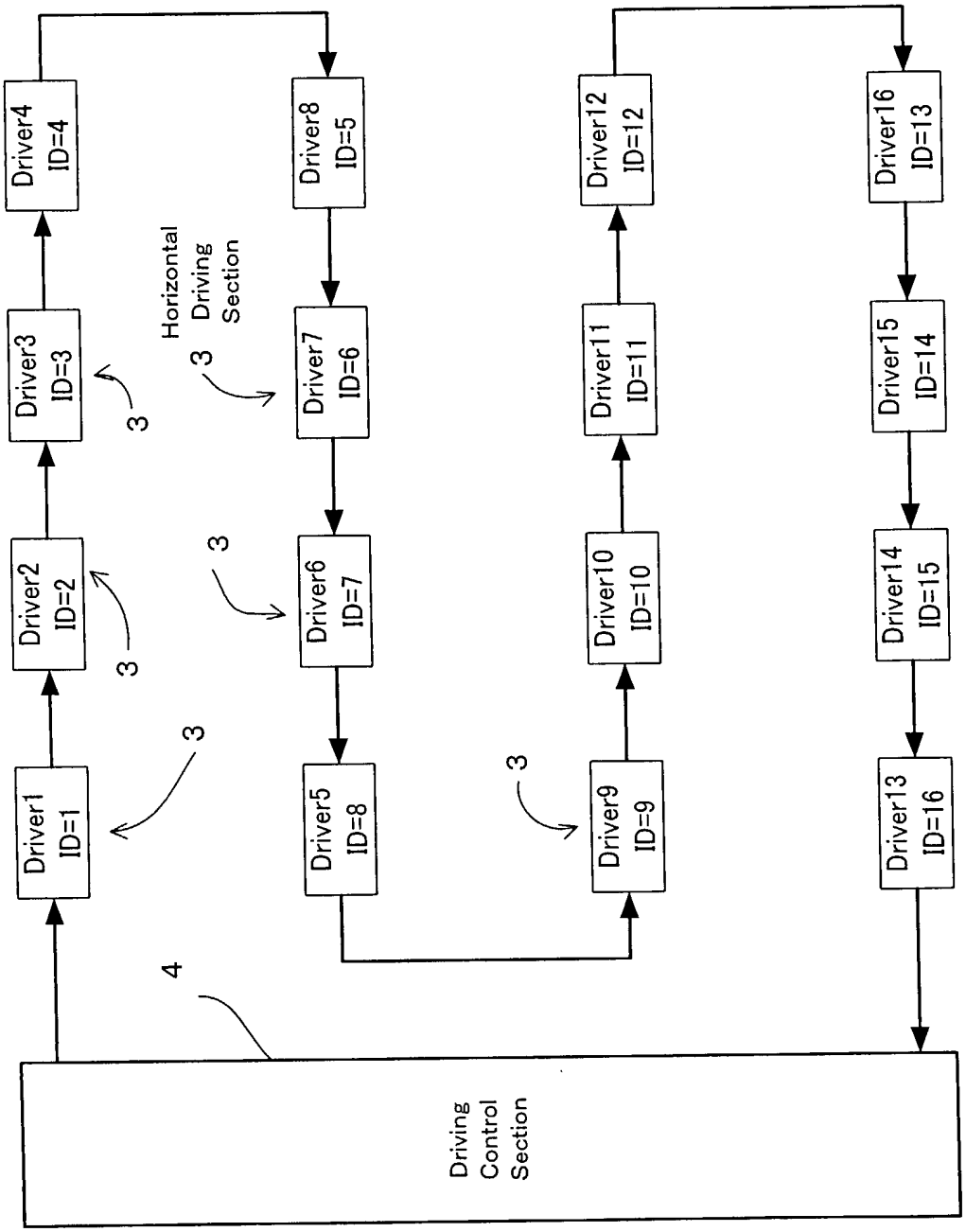
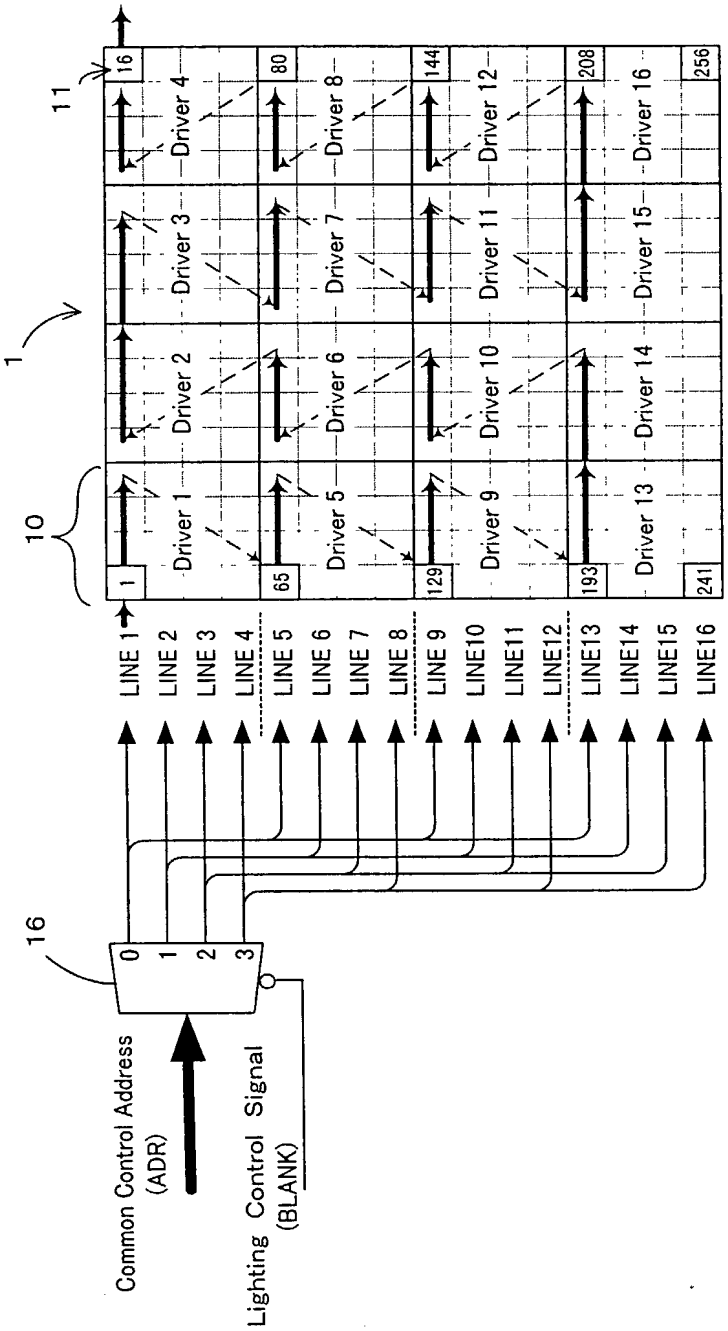

Driver1 ID=1
Driver2 ID=2
Driver3 ID=3
Driver4 ID=4
Driver5 ID=8
Driver6 ID=7
Driver7 ID=6
Driver8 ID=5
Driver9 ID=9
Driver10 ID=10
Driver11 ID=11
Driver12 ID=12
Driver13 ID=16
Driver14 ID=15
Driver15 ID=14
Driver16 ID=13
Horizontal Driving Section
3
4
Driving Control Section

FIG. 23


1
10
11
16
Driver 1
Driver 2
Driver 3
Driver 4
Driver 5
Driver 6
Driver 7
Driver 8
Driver 9
Driver 10
Driver 11
Driver 12
Driver 13
Driver 14
Driver 15
Driver 16
1
65
129
193
241
80
144
208
256
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
LINE10
LINE11
LINE12
LINE13
LINE14
LINE15
LINE16
0
1
2
3
Common Control Address (ADR)
Lighting Control Signal (BLANK)